ABSTRACT

A delay compensation circuit for a delay locked loop which includes a main delay line having a fine delay line comprising fine delay elements and a coarse delay line comprising coarse delay elements, the main delay line being controlled by a controller, the delay compensation circuit comprising: an adjustable fine delay for modeling a coarse delay element, a counter for controlling the adjustable fine delay to a value which is substantially the same as that of a coarse delay element, a circuit for applying a representation of the system clock to the delay compensation circuit, and a circuit for applying the fine delay count from the counter to the controller for adjusting the fine delay line of the main delay line to a value which is substantially the same as that of a coarse delay element of the main delay line.